MULTIMEDIA UNIVERSITY

STUDENT ID NO

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# MULTIMEDIA UNIVERSITY

# FINAL EXAMINATION

**TRIMESTER 2, 2019/2020**

## TAO1221 – COMPUTER ARCHITECTURE AND ORGANISATION

( All sections / Groups )

06 MARCH 2020
(3.00 p.m. – 5.00 p.m.)
( 2 hours )

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**INSTRUCTIONS TO STUDENTS**

1. This Question paper consists of 8 pages including cover page with 5 Questions only.

2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

## QUESTION 1

(a) Briefly describe the **FOUR(4)** components of a structure of von Neumann machine. [2 marks]

(b) Describe any **TWO(2)** characteristics of First, Second and Third Generation Computers respectively. [3 marks]

(c) Describe the content of Memory Address Register (MAR), Memory Buffer Register (MBR), Instruction Register (IR), and Program Counter (PC). [2 marks]

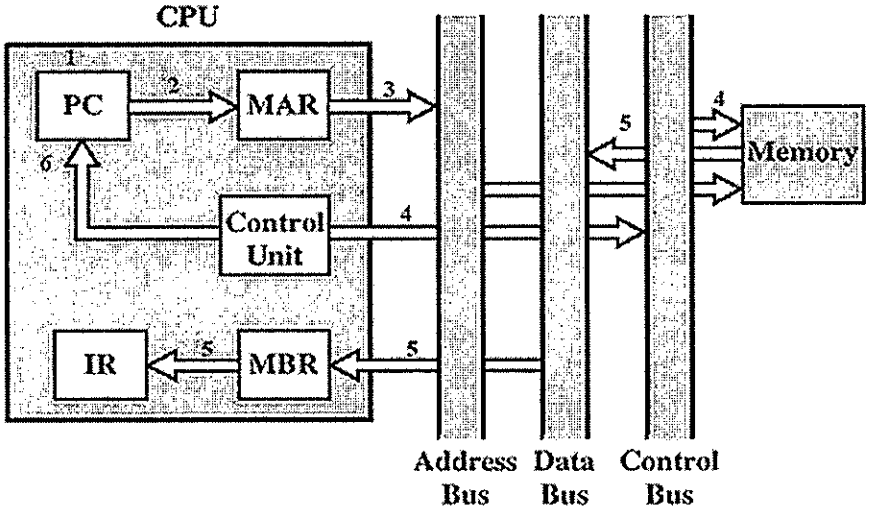
(d) Discuss **THREE(3)** key concepts of von Neumann architecture. [1.5 marks]

(e) Illustrate a basic instruction cycle, consisting fetch and execute cycle. [1.5 marks]

**Continued ....**

## QUESTION 2

(a) From the following data flow diagram, describe **SIX(6)** processes during Fetch Cycle. [3 marks]




(b) Briefly discuss **FOUR(4)** most common classes of Interrupts. [2 marks]

(c) Define Direct Memory Access (DMA). [1 mark]

(d) Assuming 8 instructions which take 45 ms to complete one execution.

i. Draw a 9-stage (FI, DI, D2, CO, FO, EI, EX, M1, W1) pipelining with 5 ms for each stage. [2 marks]

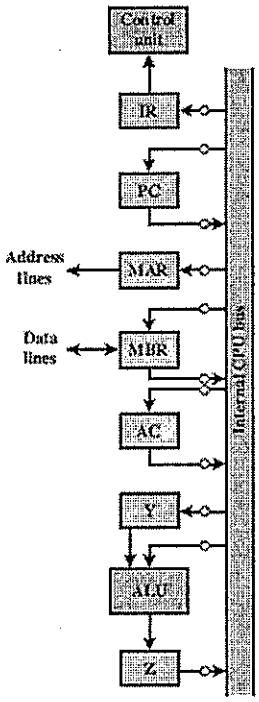
ii. Calculate the total time required to complete the execution of all the instructions without using pipelining. [1 mark]

iii. Calculate the speedup factor for the instruction pipeline compared to the execution without pipeline. [1 mark]

**Continued ....**

## QUESTION 3

(a) Referring to the bus structure given below, write the sequence of micro-operations required to add a number to the accumulator (AC) when the number is a direct-address operand. [2.5 marks]




(b) Calculate the output and determine the overflow status for the following arithmetic operations in 4-bit two's complement representation.

i. -6 + 5 [1 mark]

ii. -4 – 5 [1 mark]

(c) Referring to the flowchart provided in Appendix (Figure 1), show the steps using Booth's Algorithm for performing the multiplication of two **4-bit two's complement** binary numbers as given below: [3 marks]

Multiplicand (M) = $(0011)_2$ or $(3)_{10}$
Multiplier (Q) = $(1011)_2$ or $(-5)_{10}$

**Continued ....**

(d) Assume the usage of IEEE 32-bit format for the representation of floating-point number as given below:

| 1 | 1000 0010 | 1001 0000 0000 0000 0000 000 |
|---|---|---|
| Sign Bit (1 bit) | Biased Exponent (8 bits) | Normalized Mantissa (23 bits) |

Identify the following:

i. Biased exponent value in decimal [0.5 marks]

ii. True exponent value in decimal [0.5 marks]

iii. Sign of the number [0.5 marks]

iv. Decimal equivalent of the given 64-bit floating point number [1 mark]

**Continued ....**

## QUESTION 4

(a) A machine has the following set of instructions:

- Zero Address: PUSH M; POP M; ADD; SUB; MUL; DIV
- One-address: LOAD M; STORE M; ADD M; SUB M; MUL M; DIV M
- Two-address: MOV X, Y; ADD X, Y; SUB X, Y; MUL X, Y; DIV X, Y

Given the following expression:

$$\mathbf{X = [(G - E) * A] + [H * (A + S / L)]}$$

Write machine instruction for the machine using:

i. Zero address [2 marks]

ii. One address [2 marks]

iii. Two-address [2 marks]

(b) Describe **THREE(3)** types of addressing mode that do not need memory references. List an instruction from each category. [3 marks]

(c) Explain **TWO(2)** advantages of Symmetric Multiprocessor (SMP) over Uniprocessor. [1 mark]

**Continued ....**

## QUESTION 5

(a) A computer system has a memory architecture made up of main memory of 1GB and cache of 512KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 64 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping [3 marks]

ii. Four-way Set Associative Mapping [3 marks]

(b) Peripherals are connected to the computer through I/O modules. Explain why we do **NOT** connect the peripherals directly to the system bus. [2 marks]

(c) Describe **TWO(2)** technologies of RAM (Random Access Memory) [2 marks]

**Continued ....**

## APPENDIX

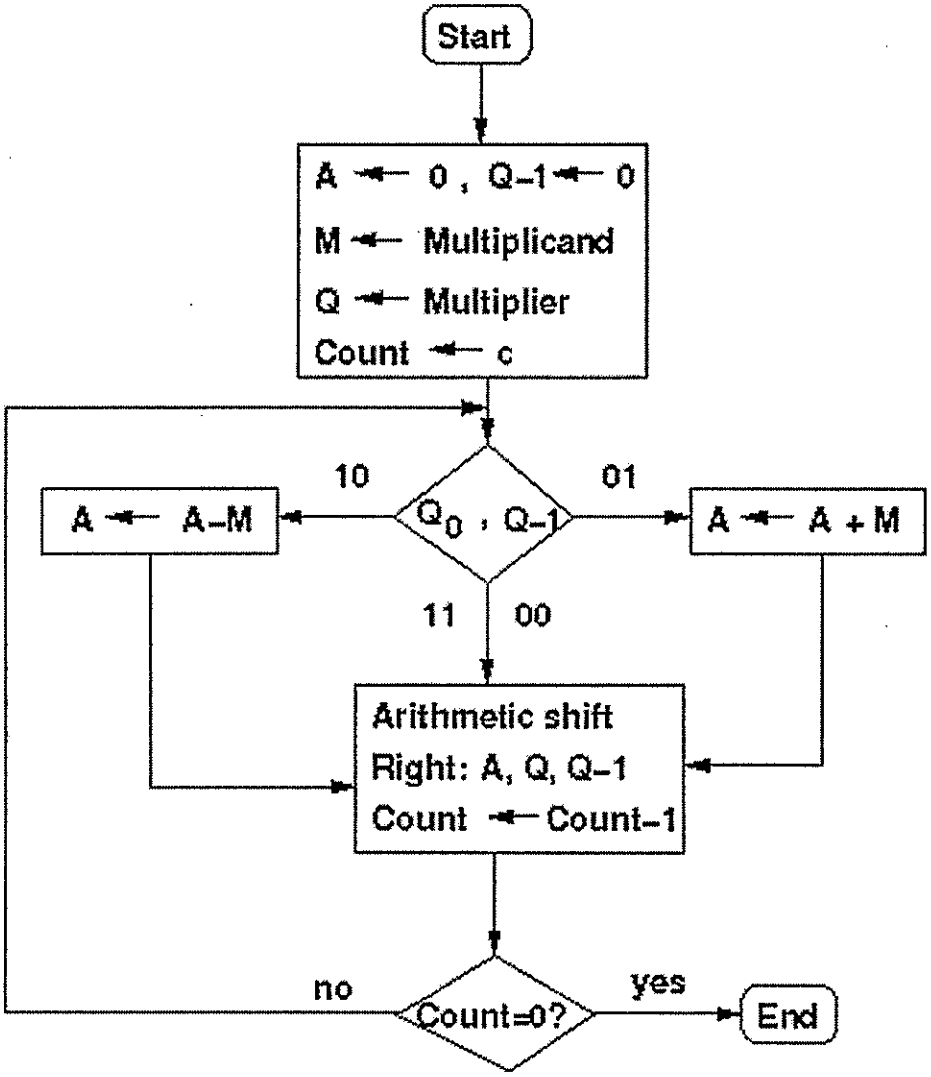



Figure 1

**End of Paper.**